PLPDI: Verification Revision Notes

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Formal Verification

This is the application of rigorous, mathematical models to establish the **correctness** of computerised systems.

Computer-aided Verification

Computer-aided verification is simply automated formal verification methods via tools and algorithms etc.

1 Labelled Transition Systems

Labelled transition systems are comprised of two parts:

- States, representing possible configurations of a systems.
 - Values of program variables
 - Values of registers in a hardware circuit
- Transitions, possible ways/routes a system can evolve
 - Execution of a program statement
 - Sequential circuit update

Formally, they can be defined as a tuple $S,Act, \rightarrow, I,AP,L$. Where:

- S is a set of states
- \bullet Act is a set of ${\bf actions}$
- $\rightarrow \subseteq$ S \times Act \times S is a transition system
- $I \subseteq S$ is a set of **initial states**
- AP is a set of **atomic propositions**
- L:S $\rightarrow 2^{AP}$ is a labelling function

1.1 Example LTS

- $S = \{ready, wait, coffee, beer\}$
- Act = {coin, press1, press2, serve}
- $\rightarrow = \{(\text{ready, coin, wait}), (\text{wait, press1, coffee}), (\text{wait, press1, beer}), (coffee, serve, ready), (beer, serve, ready)\}$
- I = {ready}
- AP = {inactive, chosen}
- L(ready) = {inactive}, L(wait) = \emptyset , L(coffee) = L(beer) = {chosen}



1.2 Labelling & Finiteness

LTS states are labelled with **atomic propositions** $a, b, \ldots \in AP$. They represent facts or observations of the system.

LTS transitions are labelled with actions $\alpha, \beta, \ldots \in Act$ and are used to communicate between *components*

An LTS is said to be *finite* if S,Act and AP are finite. We tend to assume our LTSs are finite.

1.3 Transitions

We denote transitions as $s - \alpha \rightarrow s'$ if $(s, \alpha, s') \in \rightarrow$

We define the direct successors and predecessors as:

- $\texttt{Post}(s,\alpha) = \{s\prime \in S | s \alpha \to s\prime\} \text{ and } \texttt{Post}(s) = \cup_{\alpha \in \texttt{Act}}\texttt{Post}(s,\alpha)$
- $\mathtt{Pre}(s,\alpha) = \{s\prime \in S | s\prime \alpha \to s\}$ and $\mathtt{Pre}(s) = \cup_{\alpha \in \texttt{Act}} \mathtt{Pre}(s,\alpha)$

We say that a state, s is **terminal** if $Post(s) = \emptyset$, i.e. it has no outgoing transitions. Such states can be used to represent the termination of a program or erroneous or undesired behaviour.